PATENT
Attorney Docket No. 401134/ASAHINA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TAKATA et al.

Art Unit: Unknown

Application No.: Unknown

Examiner: Unknown

Filed: March 15, 2001

For: SEMICONDUCTOR PACKAGE

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to the examination of the above-identified patent application, please enter the following amendments and consider the following remarks.

IN THE SPECIFICATION:

Replace the paragraph beginning at page 2, line 24 with:

The sealing using a resin is carried out using a mold, and the semiconductor package is pushed out of the mold using eject pins. When eject pin receiving portions 8 of the sealing resin shown in Fig. 16 are pushed up by the eject pins (not shown) so as to remove the semiconductor package from the mold, stress on the semiconductor chip is increased if the section modulus is reduced. Moreover, since the size of semiconductor chips is being reduced from year to year, resulting in a greater reduction in the sectional modulus and an increasing stress is applied to the semiconductor chip.

Replace the paragraph beginning at page 3, line 7 with:

Furthermore, the conventional semiconductor package requires a region coated with the adhesive 2 on the upper surface of the semiconductor chip 1 in order to adhere the LOC type leads 3, and the electrode pads 7 cannot be provided in the region coated with the adhesive 2. For this reason, the area on the chip 1 for arranging the electrode pads 7 is restricted to the central region (for the central electrode pads 7a) and the peripheral regions (for the peripheral electrode pads 7b) along shorter sides where the standard type leads 6 are provided. Thus, there has been a drawback in that the region on the upper surface of the semiconductor chip where the electrode pads 7 are to be provided is limited to a small I-shaped region.

Replace the paragraph beginning at page 3, line 27 with:

In the conventional semiconductor package shown in Fig. 16, the S bend of LOC type lead 3 must be located at a region in which the leads 3 are arranged rectilinearly, in parallel, in the vicinity of the outer leads 3b extending from the sealing resin. If the S bend of the LOC type lead 3 is located at a region in which the leads 3 are arranged obliquely, spacing between tips of the adjacent LOC type inner leads 3a easily becomes uneven so that the tips of the adjacent leads come in contact with each other or necessary space cannot be obtained. In the conventional semiconductor package shown in Fig. 16, leads 6 on four corners have no bent portion and other leads 3 are bent so that the leads 6 and the leads 3 are not in the same plane. Accordingly, there have been drawbacks in that a high working cost for bending is required and leads must be handled carefully so as not to be deformed.

IN THE CLAIMS:

Replace the indicated claims with:

1. (Amended) A semiconductor package comprising a semiconductor chip, a die pad, a die bond material fixing the semiconductor chip to the die pad, lead-on-chip (LOC) inner leads having tips spaced from and extending across the semiconductor chip, and metal wires connecting the tips of the LOC inner leads to electrode pads on the

semiconductor chip, sealed with a sealing resin, and outer leads extending successively from the inner leads and protruding outwardly from the sealing resin.

2. (Amended) The semiconductor package of Claim 1, including standard inner leads and metal wires connecting tips of the standard inner leads to electrode pads on the semiconductor chip are sealed with the sealing resin, and wherein

outer leads extending successively from the standard inner leads protrude outwardly from the sealing resin, and

the LOC inner leads and the standard inner leads are co-planar.

3. (Amended) The semiconductor package of claim 1, wherein a clearance between the LOC inner leads and the die pad is larger than total thickness of the semiconductor chip and the die bond material.

4. (Amended) The semiconductor package of claim 2, wherein the LOC inner leads and the standard inner leads are both arranged along at least one side of the semiconductor chip.

5. (Amended) The semiconductor package of claim 2, wherein the LOC inner leads are arranged along a first side of the semiconductor chip and the standard inner leads are arranged along a second side of the semiconductor chip.

6. (Amended) The semiconductor package of claim 1, wherein a distance between upper surfaces of the outer leads and an upper surface of the sealing resin is different from a distance between lower surfaces of the outer leads and a lower surface of the sealing resin, and ends of the die pad are exposed at opposed side surfaces of the sealing resin and lie in a plane parallel to a plane in which the outer leads protrude.

7. (Amended) A semiconductor package including at least a semiconductor chip, metal wires, lead-on-chip (LOC) inner leads having tips spaced from and extending over

the semiconductor chip, and standard inner leads having tips arranged outside of a periphery of the semiconductor chip sealed with a sealing resin, wherein

the semiconductor chip has distributed electrode pads distributed and arranged on an upper surface of the semiconductor chip and has at least either central electrode pads rectilinearly located in a central region of the semiconductor chip or peripheral electrode pads located along the periphery of the semiconductor chip, and

the LOC inner leads and the standard inner leads are co-planar and both arranged along one side of the semiconductor chip.

8. (Amended) A method of manufacturing a semiconductor package comprising:

forming a die pad frame with a die pad surrounded by a first frame,

displacing the die pad relative to the first frame,

bonding a semiconductor chip to the die pad with a die bond material,

superposing a lead frame, including inner leads surrounded by a second frame, on the die pad frame with the semiconductor chip disposed between the die pad and the inner leads,

welding the first frame and the second frame of the lead frame together,

sealing the die pad, the semiconductor chip, and the inner leads in a sealing resin, and

removing the first frame and the second frame.

IN THE ABSTRACT:

Replace the Abstract with:

Abstract of the Disclosure

A semiconductor package includes a semiconductor chip, a die pad, an adhesive, metal wires, LOC inner leads, and standard inner leads sealed within a sealing resin. The LOC inner leads and the standard inner leads are arranged in the same plane and both are arranged along one side of the semiconductor chip. Clearance between the inner leads and the die pad larger than the total thickness of the semiconductor chip and the bonding material. Thus, a semiconductor chip having

electrode pads broadly distributed can be employed and the section modulus of the semiconductor package can be increased.

REMARKS

The foregoing Amendment improves the form of the application without adding new matter.

Respectfully submitted,

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SPECIFICATION, CLAIMS AND ABSTRACT AS PRELIMINARILY AMENDED

Amendments to the paragraph beginning at page 2, line 24:

The sealing using a resin is carried out ~~by means of~~ using a mold, and the semiconductor package is ~~taken~~ pushed out of the mold ~~by means of~~ using eject pins. When eject pin receiving portions 8 of the sealing resin shown in Fig. 16 are pushed up by the eject pins (not shown) so as to remove the semiconductor package from the mold, ~~a~~ stress ~~generated~~ on the semiconductor chip is increased if the section modulus ~~of section~~ is reduced. Moreover, since the size of ~~the~~ semiconductor ~~chip~~ chips is being reduced from year to year, resulting in a ~~more~~ greater reduction in the sectional modulus ~~of section~~ and ~~a more increase in the~~ an increasing stress ~~generated on~~ is applied to the semiconductor chip.

Amendments to the paragraph beginning at page 3, line 7:

Furthermore, the conventional semiconductor package requires a region coated with the adhesive 2 on the upper surface of the semiconductor chip 1 in order to adhere the LOC type leads 3, and the electrode pads 7 cannot be provided in the region coated with the adhesive 2. For this reason, the area on the chip 1 for arranging the electrode pads 7 ~~are~~ is restricted to the central region (for the central electrode pads 7a) and the peripheral regions (for the peripheral electrode pads 7b) along shorter

sides ~~wherein~~ where the standard type leads 6 are provided. Thus, there has been a drawback in that the region on the upper surface of the semiconductor chip where the electrode pads 7 are to be provided is limited to ~~an I-shape small~~ a small I-shaped region.

Amendments to the paragraph beginning at page 3, line 27:

In the conventional semiconductor package shown in Fig. 16, the ~~bent by~~ S bend of LOC type lead 3 must be ~~formed~~ located at a region in which the leads 3 are arranged rectilinearly, in parallel, in the vicinity of the outer leads 3b ~~led~~ extending from the sealing resin. If the ~~bent~~ S bend of the LOC type lead 3 ~~are formed~~ is located at a region in which the leads 3 are arranged obliquely, ~~space~~ spacing between tips of the adjacent LOC type inner leads 3a easily ~~become~~ becomes uneven so that the tips of the adjacent leads come in contact with each other or ~~a~~ necessary space cannot be ~~taken~~ obtained. In the conventional semiconductor package shown in Fig. 16, leads 6 on four corners have no bent portion and other leads 3 are bent so that the leads 6 and the leads 3 are not ~~constituted on~~ in the same plane. Accordingly, there have been drawbacks in that a high working cost for bending is required and leads must be handled carefully so as not to be deformed.

Amendments to existing claims:

1. (Amended) A semiconductor package ~~in which~~ comprising a semiconductor chip, a die pad, a die bond material fixing the semiconductor chip ~~on~~ to the die pad, lead-on-chip (LOC) ~~type~~ inner leads having ~~their~~ tips ~~extended above~~ spaced from and extending across the semiconductor chip, and metal wires connecting the tips of the LOC ~~type~~ inner leads to electrode pads on the semiconductor chip ~~are~~, sealed with a sealing resin, ~~wherein~~ and outer leads ~~formed~~ extending successively ~~to~~ from the inner leads ~~are protruded~~ and protruding outwardly from the sealing resin.

2. (Amended) ~~A~~The semiconductor package of Claim 1, ~~in which~~ including standard ~~type~~ inner leads and metal wires connecting ~~the~~ tips of the standard ~~type~~ inner

leads to electrode pads on the semiconductor chip are ~~further~~ sealed with the sealing resin, and wherein

outer leads ~~formed~~ extending successively ~~to~~ from the standard ~~type~~ inner leads ~~are protruded~~ protrude outwardly from the sealing resin, and

the LOC ~~type~~ inner leads and the standard ~~type~~ inner leads are ~~arranged on a same plane~~ co-planar.

3. (Amended) ~~A~~The semiconductor package of claim 1, wherein a clearance between the LOC ~~type~~ inner leads and the die pad is ~~set to be~~ larger than ~~a sum of~~ total thickness of the semiconductor chip and the die bond material.

4. (Amended) ~~A~~The semiconductor package of claim 2, wherein the LOC ~~type~~ inner leads and the standard ~~type~~ inner leads are ~~mixedly~~ both arranged along at least ~~a~~ one side of the semiconductor chip.

5. (Amended) ~~A~~The semiconductor package of claim 2, wherein the LOC ~~type~~ inner leads are arranged along a first side of the semiconductor chip and the standard ~~type~~ inner leads are arranged along ~~another~~ a second side of the semiconductor chip.

6. (Amended) ~~A~~The semiconductor package of claim 1, wherein a distance between upper surfaces of the outer leads and ~~the~~ an upper surface of the sealing resin is different from a distance between lower surfaces of the outer leads and ~~the~~ a lower surface of the sealing resin, and ends of the die pad are exposed ~~in~~ at opposed side surfaces of the sealing resin and ~~being on~~ lie in a plane parallel ~~with~~ to a plane ~~on~~ in which the outer leads ~~are protruded~~ protrude.

7. (Amended) A semiconductor package ~~in which~~ including at least a semiconductor chip, metal wires, lead-on-chip (LOC) ~~type~~ inner leads having ~~their~~ tips ~~extended above~~ spaced from and extending over the semiconductor chip, and standard ~~type~~ inner leads having ~~their~~ tips arranged outside of a periphery of the semiconductor chip ~~are~~ sealed with a sealing resin, wherein

the semiconductor chip has distributed electrode pads distributed and arranged on ~~its~~ an upper surface of the semiconductor chip and has at least either central electrode pads rectilinearly ~~provided~~ located in a central region of the semiconductor chip or peripheral electrode pads ~~provided~~ located along the periphery of the semiconductor chip, and

the LOC ~~type~~ inner leads and the standard ~~type~~ inner leads are ~~arranged on a same plane~~ co-planar and ~~mixedly~~ both arranged along ~~a~~ one side of the semiconductor chip.

8. (Amended) A method of manufacturing a semiconductor package comprising~~:~~:

forming a die pad frame ~~in which~~ with a die ~~pads are~~ pad surrounded ~~with~~ by a first frame,

~~depressing~~displacing the die pad ~~to make a displacement between the die pad and the frame~~ relative to the first frame,

bonding a semiconductor chip to the die pad with a die bond material,

superposing a lead frame, ~~in which~~ including inner leads ~~are~~ surrounded ~~with~~ by a second frame, on the die pad frame ~~so as to interpose~~ with the semiconductor chip disposed between the die ~~pads~~ pad and the inner leads,

welding the first frame ~~of the die pad~~ and the second frame of the lead frame together,

sealing the die pad, the semiconductor chip, and the inner leads ~~with~~ in a sealing resin, and

removing the first frame ~~of the die pad~~ and the second frame ~~of the lead frame away~~.

Amendments to the abstract:

Abstract of the Disclosure

~~The present invention provides a~~A semiconductor package ~~in which~~ includes a semiconductor chip, a die pad, an adhesive, metal wires, LOC ~~type~~ inner leads, and standard ~~type~~ inner leads ~~are~~ sealed ~~with~~ within a sealing resin. The LOC ~~type~~ inner leads and the standard ~~type~~ inner leads are arranged ~~on a~~ in the same plane and ~~mixedly~~ both are arranged along ~~a~~ one side of the semiconductor chip. Clearance

between the inner leads and the die pad ~~is set to be~~ larger than ~~a sum of~~ the total thickness of the semiconductor chip and the bonding material. Thus, a semiconductor chip having electrode pads broadly distributed ~~and arranged thereon~~ can be employed and the section modulus ~~of section~~ of the semiconductor package can be ~~enhanced~~ increased.

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CLAIMS PENDING AFTER PRELIMINARY AMENDMENT

1. A semiconductor package comprising a semiconductor chip, a die pad, a die bond material fixing the semiconductor chip to the die pad, lead-on-chip (LOC) inner leads having tips spaced from and extending across the semiconductor chip, and metal wires connecting the tips of the LOC inner leads to electrode pads on the semiconductor chip, sealed with a sealing resin, and outer leads extending successively from the inner leads and protruding outwardly from the sealing resin.

2. The semiconductor package of Claim 1, including standard inner leads and metal wires connecting tips of the standard inner leads to electrode pads on the semiconductor chip are sealed with the sealing resin, and wherein

outer leads extending successively from the standard inner leads protrude outwardly from the sealing resin, and

the LOC inner leads and the standard inner leads are co-planar.

3. The semiconductor package of claim 1, wherein a clearance between the LOC inner leads and the die pad is larger than total thickness of the semiconductor chip and the die bond material.

4. The semiconductor package of claim 2, wherein the LOC inner leads and the standard inner leads are both arranged along at least one side of the semiconductor chip.

5. The semiconductor package of claim 2, wherein the LOC inner leads are arranged along a first side of the semiconductor chip and the standard inner leads are arranged along a second side of the semiconductor chip.

6. The semiconductor package of claim 1, wherein a distance between upper surfaces of the outer leads and an upper surface of the sealing resin is different from a distance between lower surfaces of the outer leads and a lower surface of the sealing resin, and ends of the die pad are exposed at opposed side surfaces of the sealing resin and lie in a plane parallel to a plane in which the outer leads protrude.

7. A semiconductor package including at least a semiconductor chip, metal wires, lead-on-chip (LOC) inner leads having tips spaced from and extending over the semiconductor chip, and standard inner leads having tips arranged outside of a periphery of the semiconductor chip sealed with a sealing resin, wherein

the semiconductor chip has distributed electrode pads distributed and arranged on an upper surface of the semiconductor chip and has at least either central electrode pads rectilinearly located in a central region of the semiconductor chip or peripheral electrode pads located along the periphery of the semiconductor chip, and

the LOC inner leads and the standard inner leads are co-planar and both arranged along one side of the semiconductor chip.

8. A method of manufacturing a semiconductor package comprising:

forming a die pad frame with a die pad surrounded by a first frame,

displacing the die pad relative to the first frame,

bonding a semiconductor chip to the die pad with a die bond material,

superposing a lead frame, including inner leads surrounded by a second frame, on the die pad frame with the semiconductor chip disposed between the die pad and the inner leads,

welding the first frame and the second frame of the lead frame together,

sealing the die pad, the semiconductor chip, and the inner leads in a sealing resin, and

removing the first frame and the second frame.